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10/806,301	03/22/2004	Jae-Yoon Yoo	SAM-0564	1809

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,301	YOO ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-24 and 26-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34-45* is/are allowed.

6)☒ Claim(s) *1-3,8,11-16,18-20 and 27-32* is/are rejected.

7)☒ Claim(s) *4-7,10,17,21-24,26 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Amendment filed 8/12/2005.

Currently, claim 1-8, 10-24 and 26-45 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-3, 8, 11-16, 18-20 and 27-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (U.S. Patent No. 6,518,155, filed 6/30/1997) in view of Maszara et al. (U.S. Patent No. 6, 362,063 dated 3/26/2002).

Chau shows the method as claimed in Figs. 3A-3I and corresponding text as: forming an insulated gate pattern on a semiconductor substrate (300), the insulated gate pattern (301) including a silicon pattern (320) and a sacrificial layer pattern (322) sequentially stacked (col. 5, line 47-col. 6, line 20); forming spacers (330) covering sidewalls of the gate pattern (col. 6, line 32-46); injecting impurity ions into the

semiconductor substrate using the spacers and the gate pattern as ion injection masks to form source/drain regions (331, 333)(col. 7, lines 7-23); removing the sacrificial layer pattern on the semiconductor substrate having the source/drain regions to expose the silicon pattern (col. 7, lines 7-23); and converting the exposed silicon pattern into a gate silicide layer, and concurrently selectively forming source/drain silicide layers at surfaces of the source/drain regions (col. 7, lines 51-67) (claim 1). Chau teaches that the semiconductor substrate is one of a single crystal silicon substrate, a silicon-on-insulator (SOI) substrate, and a strained silicon substrate (col. 4, line 66-col. 5, line 10) (claim 2). Chau teaches that sequentially forming a gate insulating layer and a silicon layer on the semiconductor substrate (col. 5, lines 11-67); forming a sacrificial layer on the semiconductor substrate having the silicon layer; and sequentially patterning the sacrificial layer and the silicon layer (col. 6, lines 1-20) (claim 3). Chau teaches doping the silicon layer on top of the semiconductor substrate with impurities to control a threshold voltage (col. 7, lines 7-23) (claim 8). Chau teaches that the spacers are formed of an insulating layer having an etch selectivity with respect to the sacrificial layer pattern (col. 6, lines 32-46) (claim 11). Chau teaches that the insulating layer having the etch selectivity is composed of multiple layers including a silicon oxide layer and a silicon nitride layer (col. 6, lines 32-46) (claim 12). Chau teaches that a metal layer (334) is formed on the semiconductor substrate having the exposed silicon pattern (col. 7, lines 24-34); annealing the metal layer until the exposed silicon pattern is silicided (col. 7, lines 35-50) and removing the unreacted portion of the metal layer remaining on the spacers (col. 7, lines 35-50) (claim 13). Chau teaches that the metal

layer comprises at least one metal layer comprising a metal selected from the group consisting of Ni, Co, W, and Ti (col. 7, lines 24-34) (claim 14). Chau teaches that the metal layer comprises an alloy of a metal selected from the group consisting of Ni, Co, W, and Ti (col. 7, lines 24-34) (claim 15). Chau teaches that the metal layer is one of nickel layer and a nickel alloy layer (col. 8, lines 1-8) (claim 16). Chau shows the method as claimed in Figs. 3A-3I and corresponding text as: defining an NMOS transistor region (314) and a PMOS transistor region (316) on a predetermined portion of a semiconductor substrate (col. 5, lines 47-49); forming insulated gate patterns on the NMOS transistor region and the PMOS transistor region, each of the insulated gate patterns including a silicon pattern and a sacrificial layer pattern sequentially stacked (col. 6, lines 1-20); forming spacers covering sidewalls of the gate patterns (col. 6, lines 32-46); injecting impurity ions into the NMOS transistor region and the PMOS transistor region using the gate patterns and the spacers as ion injection masks to form source/drain regions (col. 7, lines 7-23); removing the sacrificial layer patterns on the semiconductor substrate having the source/drain regions to expose the silicon patterns (col. 7, lines 7-23); and converting the exposed silicon patterns into gate silicide layers, and concurrently selectively forming source/drain silicide layers at surfaces of the source/drain regions (col. 7, lines 35-50) (claim 18). Chau teaches that the semiconductor substrate is one of a single crystal silicon substrate, a silicon-on-insulator (SOI) substrate, and a strained silicon substrate (col. 4, line 66-col. 5, line 10) (claim 19). Chau teaches that sequentially forming a gate insulating layer and a silicon layer on the semiconductor substrate (col. 5, lines 11-67); forming a sacrificial layer on

the semiconductor substrate having the silicon layer; and sequentially patterning the sacrificial layer and the silicon layer (col. 6, lines 1-20) (claim 20). Chau teaches that the spacers are formed of an insulating layer having an etch selectivity with respect to the sacrificial layer pattern (col. 6, lines 32-46) (claim 27). Chau teaches that the insulating layer having the etch selectivity is composed of multiple layers including a silicon oxide layer and a silicon nitride layer (col. 6, lines 32-46) (claim 28). Chau teaches that a metal layer (334) is formed on the semiconductor substrate having the exposed silicon pattern (col. 7, lines 24-34); annealing the metal layer until the exposed silicon pattern is silicided (col. 7, lines 35-50) and removing the unreacted portion of the metal layer remaining on the spacers (col. 7, lines 35-50) (claim 29). Chau teaches that the metal layer comprises at least one metal layer comprising a metal selected from the group consisting of Ni, Co, W, and Ti (col. 7, lines 24-34) (claim 30). Chau teaches that the metal layer comprises an alloy of a metal selected from the group consisting of Ni, Co, W, and Ti (col. 7, lines 24-34) (claim 31). Chau teaches that the metal layer is one of nickel layer and a nickel alloy layer (col. 8, lines 1-8) (claim 32).

Chau lacks anticipation only in not explicitly teaching that: 1) impurity ions are injected into the semiconductor substrate using the gate pattern as an ion injection mask to form an LDD of a first conductivity type and a halo of a second conductivity type prior to formation of the spacers (claim 1); and 2) impurity ions are injected into the NMOS transistor region and the PMOS transistor region on the semiconductor substrate using the gate patterns as an ion injection mask to form LDDs of a first conductivity type in the NMOS region and a second conductivity type in the PMOS region and halos of

the second conductivity type in the NMOS region and the first conductivity in the PMOS region prior to formation of the spacers (claim 18).

Maszara shows the formation of low thermal budget shallow abrupt junctions for semiconductor devices. Maszara shows the formation of the halo implant, and an n-type dopant is implanted into the substrate (302) to form an inactive dopant region (402) to form n-type halo region (406) (col. 7, lines 11-25). This process helps to reduce horizontal and vertical dimensions of devices (col. 1, lines 12-18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the teachings of Chau by injecting impurity ions into a semiconductor substrate prior to spacer formation, as taught by Maszara, with the motivation that Maszara shows a method that helps to reduce horizontal and vertical dimensions of devices.

Allowable Subject Matter

4. Claims 34-45 are allowed.

5. Claims 4-7, 10, 17, 21-24, 26 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...further comprising doping the silicon layer with impurities to control a threshold voltage prior to formation of the sacrificial layer, as required by claim 4, as it depends from claim 3;

...further comprising forming offset spacers covering the sidewalls of the gate pattern prior to formation of the LDD and the halo, as required by claims 10 and 26, as it depends from claims 9 and 25 respectively;

...further comprising forming a selective epitaxial growth layer on the source/drain regions before removing the sacrificial layer pattern, as required by claims 17 and 33, as it depends on claims 1 and 18, respectively;

... further comprising doping the silicon layer on the upper portion of the NMOS transistor region and the PMOS transistor region with impurities to control a threshold voltage prior to formation of the sacrificial layer, as required by claim 21, as it depends from claim 20; and

...further comprising injecting impurity ions into the NMOS transistor region and the PMOS transistor region on the semiconductor substrate using the gate patterns as an ion injection mask to form LDDs and halos prior to formation of the spacers, as required by claim 24 as it depends from claim 20.

Response to Arguments

7. Applicant's arguments with respect to claims 1 and 18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
October 28, 2005